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July 2014

FL7733
Primary-Side-Regulated LED Driver with Power Factor Correction

Features

High Performance

- Cost-Effective Solution without Requiring Input Bulk Capacitor and Secondary Feedback Circuitry
- Power Factor Correction
- THD <10% Over Universal Line Range
- Constant Current Tolerance:
  - < ±1% Over Universal Line Voltage Variation
  - < ±1% by 50% - 100% Load Voltage Variation
  - < ±1% by ±20% Magnetizing Inductance Variation
- High-Voltage Startup with V_{DD} Regulation
- Adaptive Feedback Loop Control for Startup without Overshoot

High Reliability

- LED Short / Open Protection
- Output Diode Short Protection
- Sensing Resistor Short / Open Protection
- V_{DD} Over-Voltage Protection (OVP)
- V_{DD} Under-Voltage Lockout (UVLO)
- Over-Temperature Protection (OTP)
- All Protections are Auto Restart (AR)
- Cycle-by-Cycle Current Limit
- Application Input Voltage Range: 80 V_{AC} - 308 V_{AC}

Applications

- LED Lighting System

Description

This highly integrated PWM controller with advanced Primary-Side Regulation (PSR) technique provides features to enhance the performance of low-to-mid-power LED lighting converter. The FL7733 LED driver is designed with minimum system components while LED current is accurately controlled by Fairchild's TRUECURRENT® technique and improved feedback loop control. Constant Current (CC) tolerance less than ±1% over the universal line voltage range meets the requirement of highly reliable LED brightness management.

By minimizing turn-on time fluctuation, high power factor, and low THD; <10% THD over the universal line range can be obtained. An integrated high-voltage startup circuit implements fast startup and high system efficiency. During startup, adaptive feedback loop control anticipates the steady-state condition and sets initial feedback condition close to the steady state to ensure no overshoot or undershoot of LED current.

The FL7733 provides powerful protections, such as LED short / open, output diode short, sensing resistor short / open, and over-temperature for high system reliability.

The FL7733 controller is available in an 8-pin Small-Outline Package (SOP).

Related Resources

AN-5076 — Design High Power Factor Flyback Converter using FL7733 for LED Driver with Ultra-Wide Output Voltage

AN-FEBFL7733_L50U008A — User Guide for FEBFL7733_L50U008A Evaluation Board of 8.4 W LED Driver (PFC PSR Flyback)

AN-FEBFL7733_L52U050A — User Guide for FEBFL7733_L52U050A Evaluation Board of 50 W LED Driver (PFC PSR Flyback)

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FL7733MX	-40°C to +125°C	8-Lead, Small Outline Package (SOP-8)	Tape & Reel

Application Diagram

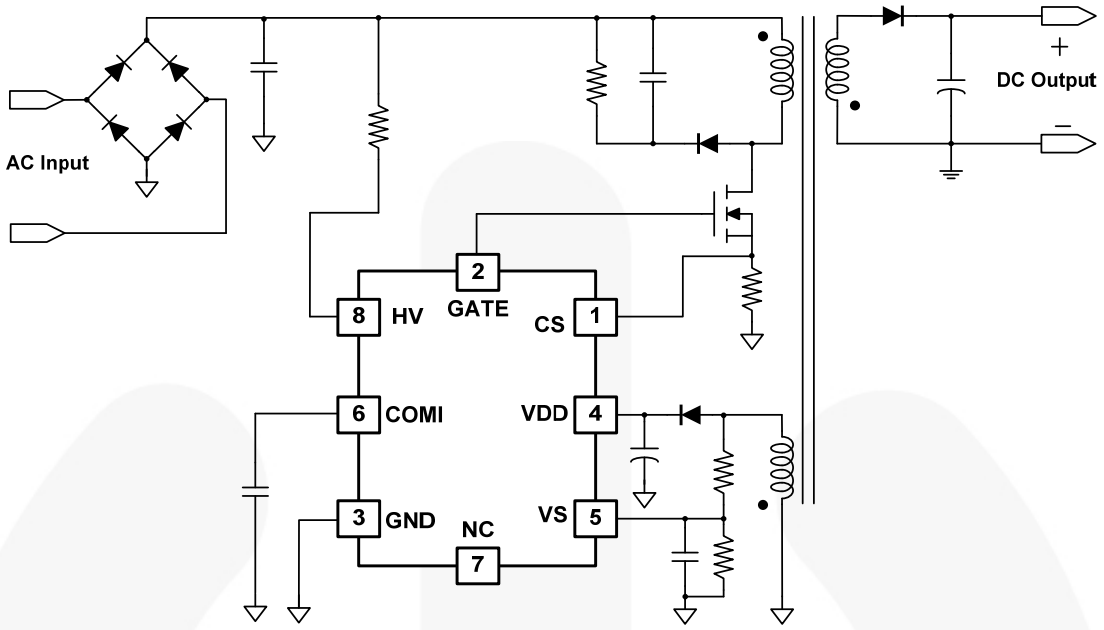


Figure 1. Typical Application

Block Diagram

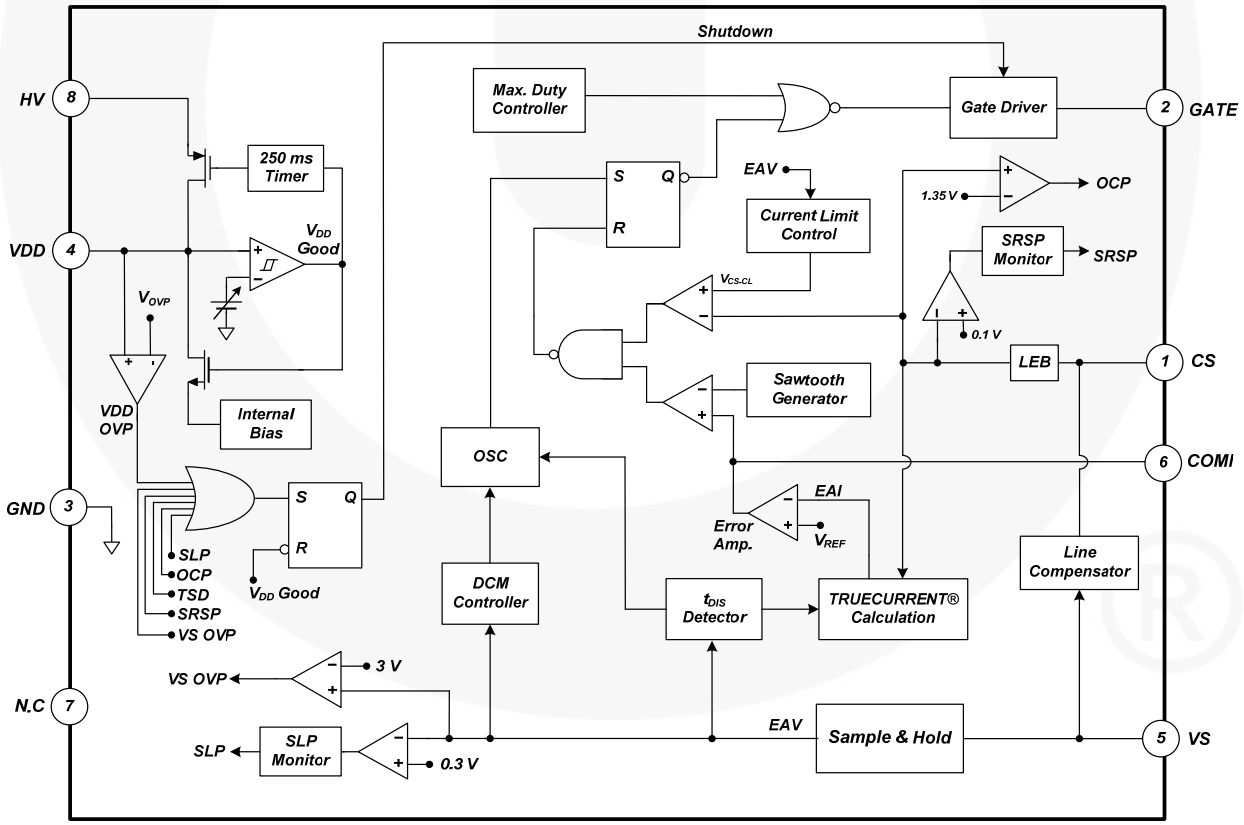
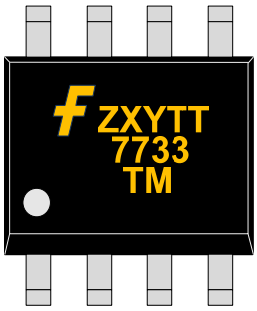


Figure 2. Functional Block Diagram

Marking Information



F: Fairchild Logo
Z: Plant Code
X: 1-Digit Year Code
Y: 1-Digit Week Code
TT: 2-Digit Die Run Code
T: Package Type (M=SOP)
M: Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

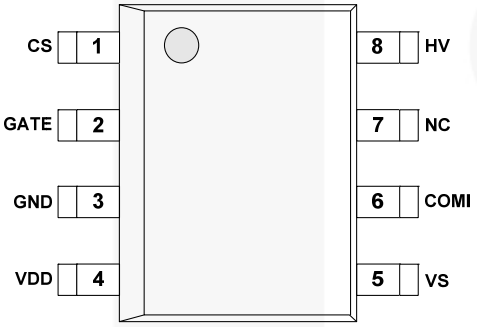


Figure 4. Pin Configuration (Top View)

Pin Descriptions

Pin #	Name	Description
1	CS	**Current Sense**. This pin connects a current-sense resistor to detect the MOSFET current for constant output current regulation.
2	GATE	**PWM Signal Output**. This pin uses the internal totem-pole output driver to drive the power MOSFET.
3	GND	**Ground**
4	VDD	**Power Supply**. IC operating current and MOSFET driving current are supplied using this pin.
5	VS	**Voltage Sense**. This pin detects the output voltage and discharge time information for CC regulation. This pin is connected to the auxiliary winding of the transformer via a resistor divider.
6	COMI	**Constant Current Loop Compensation**. This pin is connected to a capacitor between COMI and GND for compensating the current loop gain.
7	NC	No Connect
8	HV	**High Voltage**. This pin is connected to the rectified input voltage via a resistor.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
HV	HV Pin Voltage		700	V
V_{VDD}	DC Supply Voltage[1,2]		30	V
V_{VS}	VS Pin Input Voltage	-0.3	6.0	V
V_{CS}	CS Pin Input Voltage	-0.3	6.0	V
V_{COMI}	COMI Pin Input Voltage	-0.3	6.0	V
V_{GATE}	GATE Pin Input Voltage	-0.3	30.0	V
P_D	Power Dissipation ($T_A < 50°C$)		633	mW
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	-55	150	°C
T_L	Lead Temperature (Soldering) 10 Seconds		260	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.

Thermal Impedance

T_A=25°C, unless otherwise specified

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance	158	°C/W
θ_{JC}	Junction-to-Case Thermal Impedance	39	°C/W

Note:

3. Referenced the JEDEC recommended environment, JESD51-2, and test board, JESD51-3, 1S1P with minimum land pattern.

ESD Capability

Symbol	Parameter	Value	Unit
ESD	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	4	kV
	Charged Device Model, JESD22-C101	2	

Note:

4. Meets JEDEC standards JESD22-A114 and JESD 22-C101.

Electrical Characteristics

V_{DD}=15 V, T_J=-40 to +125°C, unless otherwise specified. Currents are defined as positive into the device and negative out of device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD-ON}	Turn-On Threshold Voltage		14.5	16.0	17.5	V
V_{DD-OFF}	Turn-Off Threshold Voltage		6.75	7.75	8.75	V
I_{DD-OP}	Operating Current	C_L=1 nF, f=f_{MAX-CC}	3	4	5	mA
I_{DD-ST}	Startup Current	V_{DD}=V_{DD-ON}–1.6 V		30	50	µA
$V_{VDD-OVP}$	V_{DD} Over-Voltage Protection Level		23	24	25	V
GATE SECTION						
V_{OL}	Output Voltage Low	T_A=25°C, V_{DD}=20 V, I_{DD_GATE}=1 mA			1.5	V
V_{OH}	Output Voltage High	T_A=25°C, V_{DD}=10 V, I_{DD}=1 mA	5			V
I_{SOURCE}	Peak Sourcing Current(5)	V_{DD}=10 ~ 20 V		-60		mA
I_{SINK}	Peak Sinking Current(5)	V_{DD}=10 ~ 20 V		180		mA
t_R	Rising Time	T_A=25°C, V_{DD}=15 V, C_{LOAD} =1 nF	100	150	200	ns
t_F	Falling Time	T_A=25°C, V_{DD}=15 V, C_{LOAD}=1 nF	20	60	100	ns
V_{CLAMP}	Output Clamp Voltage	V_{DD}=20 V, V_{CS}=0 V, V_{VS}=0 V, V_{COM}=0 V	12	15	18	V
HV STARTUP SECTION						
I_{HV}	Supply Current From HV Pin	T_A=25°C, V_{IN}=90 V_{AC}, V_{DD} =0 V			9	mA
I_{HV-LC}	Leakage Current after Startup			1	10	µA
t_{R-JFET}	JFET Regulation Time after Startup(5)	T_A=25°C	190	250	310	ms
$V_{JFET-HL}$	JFET Regulation High Limit Voltage		17.5	19.0	20.5	V
$V_{JFET-LL}$	JFET Regulation Low Limit Voltage		11.5	13.0	14.5	V
CURRENT-ERROR-AMPLIFIER SECTION						
g_M	Transconductance(5)	T_A=25°C	11	17	23	µmho
$I_{COMI-SINK}$	COMI Sink Current	T_A=25°C, V_{EAI}=2.55 V, V_{COMI}=5 V	12	18	24	µA
$I_{COMI-SOURCE}$	| COMI Source Current |	T_A=25°C, V_{EAI}=0.45 V, V_{COMI}=0 V	12	18	24	µA
$V_{COMI-HGH}$	COMI High Voltage	V_{EAI}=0 V	4.7			V
$V_{COMI-LOW}$	COMI Low Voltage	V_{EAI}=5 V			0.1	V
$V_{COMI\_INT.CLP}$	Initial COMI Clamping Voltage(5)			1.2		V
$t_{COMI\_INT.CLP}$	Time for Initial COMI Clamping(5)			15		ms

Continued on the following page…

Electrical Characteristics (Continued)

V_{DD}=15 V, T_J=-40 to +125°C, unless otherwise specified. Currents are defined as positive into the device and negative out of device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VOLTAGE-SENSE SECTION						
$V_{VS-MAX-CC}$	V_S for Maximum Frequency in CC	f=f_{MAX-CC}–2 kHz	2.25	2.35	2.45	V
$V_{VS-MIN-CC}$	V_S for Minimum Frequency in CC	f=f_{MIN-CC}+2 kHz	0.55	0.85	1.15	V
$t_{DIS-BNK}$	t_{DIS} Blanking Time of V_S[5]		0.85	1.15	1.45	µs
I_{VS-BNK}	V_S Current for VS Blanking		-75	-90	-105	µA
V_{VS-OVP}	V_S Level for Output Over-Voltage Protection		2.95	3.00	3.15	V
$V_{VS-LOW-CL-EN}$	V_S Threshold Voltage to Enable Low Current Limit[5]		0.25	0.30	0.35	V
$V_{VS-HIGH-CL-DIS}$	V_S Threshold Voltage to Disable Low Current Limit[5]		0.54	0.60	0.66	V
$V_{VS-SLP-TH}$	V_S Threshold Voltage for Output Short-LED Protection		0.25	0.30	0.35	V
$t_{SLP-BNK}$	V_S Detection Disable Time after Startup[5]	T_A=25°C		15		ms
CURRENT-SENSE SECTION						
V_{RV}	Reference Voltage	T_A=25°C	1.485	1.500	1.515	V
t_{LEB}	Leading-Edge Blanking Time[5]			300		ns
t_{MIN}	Minimum On Time in CC[5]	V_{COMI}=0 V		500		ns
t_{PD}	Propagation Delay to GATE Output		50	100	150	ns
$V_{CS-HIGH-CL}$	High Current Limit Threshold		0.9	1.0	1.1	V
$V_{CS-LOW-CL}$	Low Current Limit Threshold		0.16	0.20	0.24	V
t_{LOW-CM}	Low Current Mode Operation Time at Startup[5]			20		ms
$V_{CS-SRSP}$	V_{CS} Threshold Voltage for Sensing Resistor Short Protection				0.1	V
V_{CS-OCP}	V_{CS} Threshold Voltage for Over-Current Protection	T_A=25°C	1.20	1.35	1.50	V
V_{CS} / I_{VS}	Relation of Line Compensation Voltage and V_S Current[5]			21.5		V/A
OSCILLATOR SECTION						
f_{MAX-CC}	Maximum Frequency in CC	T_A=25°C, V_{DD}=10 V, 20 V	60	65	70	kHz
f_{MIN-CC}	Minimum Frequency in CC	T_A=25°C, V_{DD}=10 V, 20 V	21.0	23.5	26.0	kHz
t_{ON-MAX}	Maximum Turn-On Time	T_A=25°C, f=f_{MAX-CC}	10.4	13.0	15.6	µs
OVER-TEMPERATURE-PROTECTION SECTION						
T_{OTP}	Threshold Temperature for OTP[5]			150		°C
$T_{OTP-HYS}$	Restart Junction Temperature Hysteresis[5]			10		°C

Note:

5. These parameters, although guaranteed by design, are not production tested.

Typical Performance Characteristics

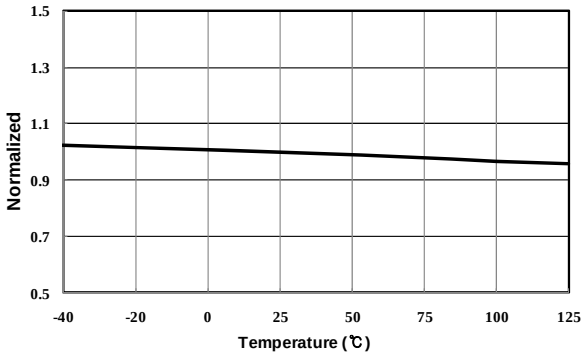


Figure 5. V_{DD-ON} vs. Temperature

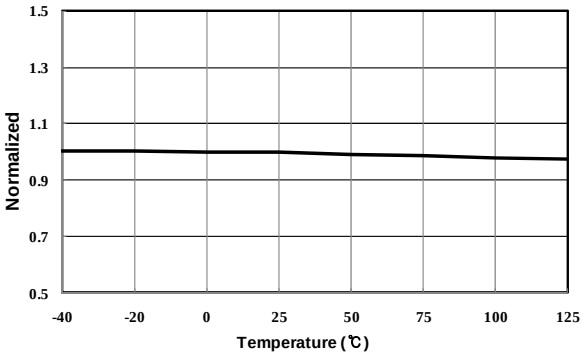


Figure 6. V_{DD-OFF} vs. Temperature

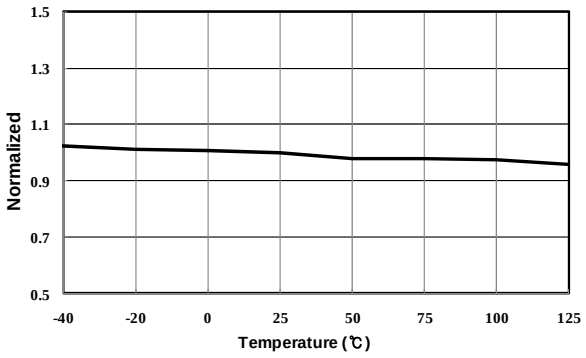


Figure 7. I_{DD-OP} vs. Temperature

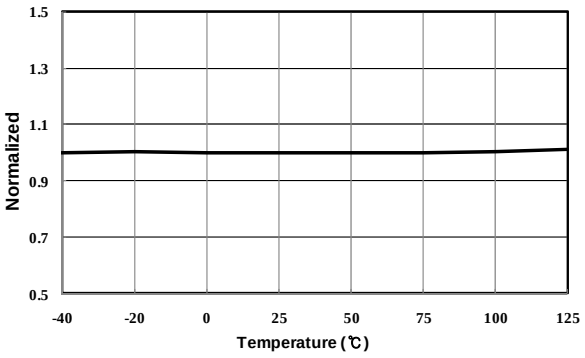


Figure 8. V_{DD-OVP} vs. Temperature

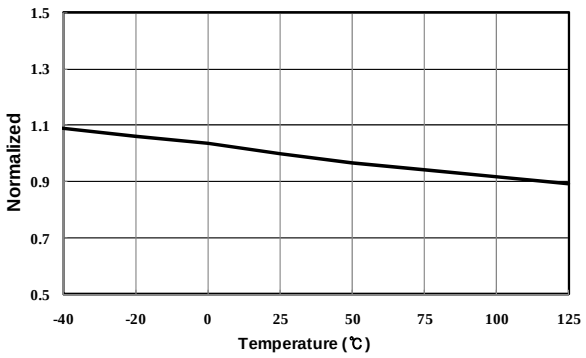


Figure 9. f_{MAX-CC} vs. Temperature

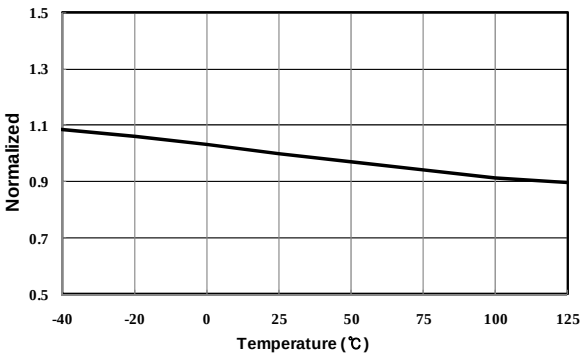


Figure 10. f_{MIN-CC} vs. Temperature

Typical Performance Characteristics (Continued)

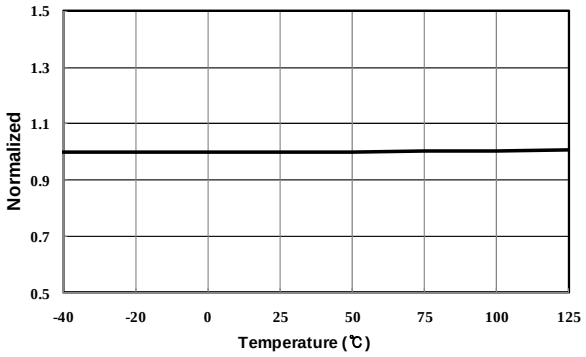


Figure 11. V_{VR} vs. Temperature

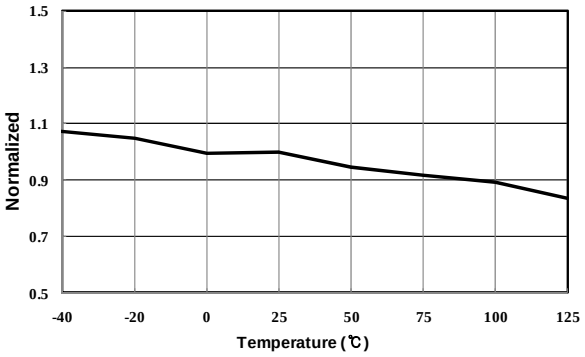


Figure 12. Gm vs. Temperature

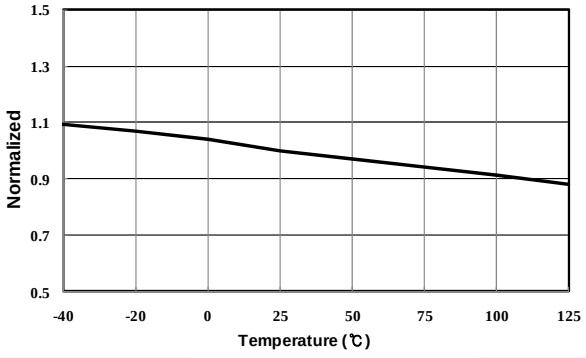


Figure 13. $I_{COMI-SOURCE}$ vs. Temperature

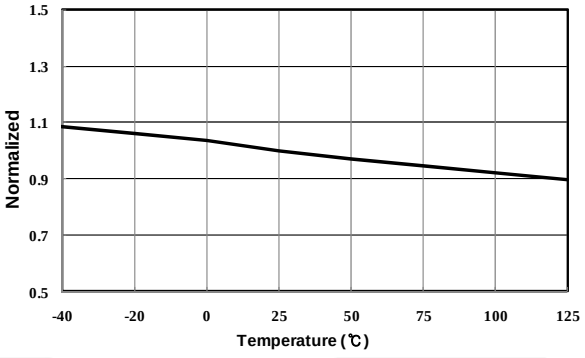


Figure 14. $I_{COMI-SINK}$ vs. Temperature

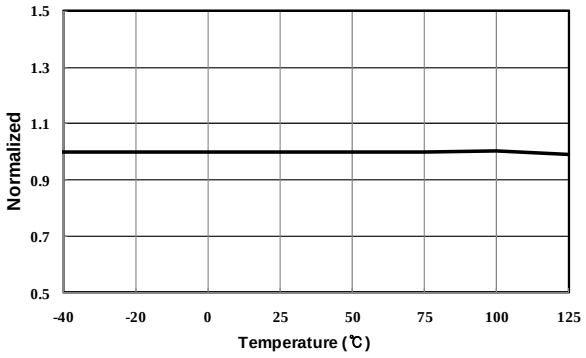


Figure 15. V_{VS-OVP} vs. Temperature

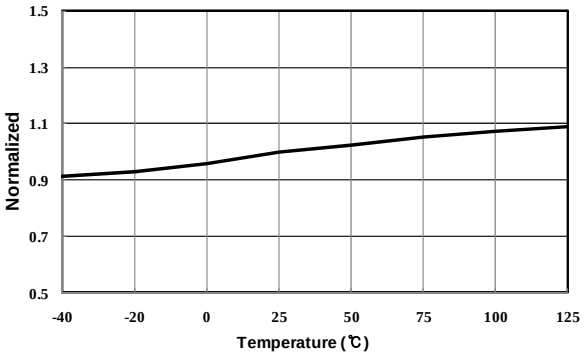


Figure 16. V_{CS-OCP} vs. Temperature

Functional Description

FL7733 is AC-DC PWM controller for LED lighting applications. TRUECURRENT® techniques regulate accurate constant LED current; independent of input voltage, output voltage, and magnetizing inductance variations. The DCM control in the oscillator reduces conduction loss and maintains DCM operation over a wide range of output voltage, which implements high power factor correction in a single-stage flyback or buck-boost topology. A variety of protections, such as LED short / open protection, sensing resistor short / open protection, over-current protection, over-temperature protection, and cycle-by-cycle current limitation stabilize system operation and protect external components.

Startup

At startup, an internal high-voltage JFET supplies startup current and V_{DD} capacitor charging current, as shown in Figure 17. When V_{DD} reaches 16 V, switching begins and the internal high-voltage JFET continues to supply V_{DD} operating current for an initial 250 ms to maintain V_{DD} voltage higher than V_{DD-OFF}. As the output voltage increases, the auxiliary winding becomes the dominant V_{DD} supply current source.

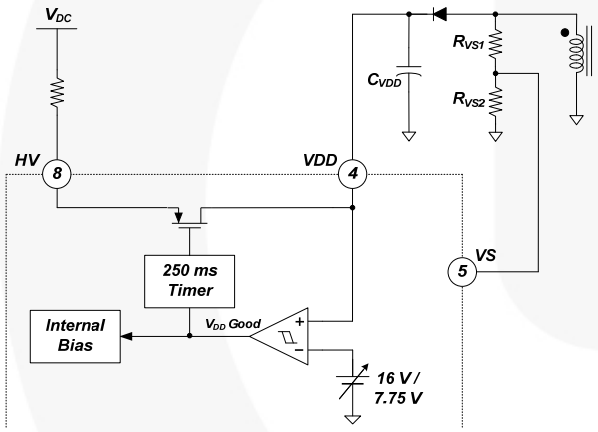


Figure 17. Startup Block

Switching is controlled by current-mode for 20 ms after V_{DD-ON}. During current-mode switching with the flyback or buck-boost topology, output current is only determined by output voltage. Therefore, the output voltage increases with constant slope, regardless of line voltage variation. Short-LED Protection (SLP) is enabled after the 15 ms SLP blanking time so that the output voltage is higher than SLP threshold voltage and successful startup is guaranteed without SLP in normal condition.

During current-mode switching, COMI voltage, which determines turn-on time in voltage mode, is adjusted close to the steady state level by sensing peak line voltage. The COMI capacitor is charged to 1.2 V for 15 ms and adjusted to a modulated level inversely proportional to V_{IN} peak value for 5 ms. Turn-on time right after 20 ms startup time can be controlled close to steady state on time so that voltage mode is smoothly entered without LED current overshoot or undershoot.

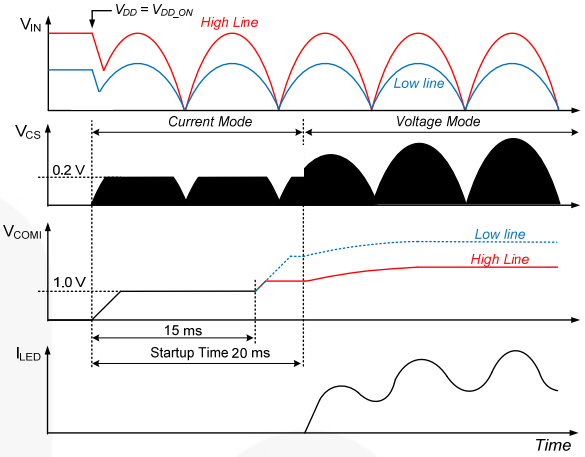


Figure 18. Startup Sequence

PFC and THD

In the flyback or the buck-boost topology, constant turn-on time and constant frequency in Discontinuous Conduction Mode (DCM) operation can achieve high PF and low THD, as shown in Figure 19. Constant turn-on time is maintained by the internal error amplifier and a large external COMI capacitor (typically over 1 µF) at COMI pin. Constant frequency and DCM operation are managed by DCM control.

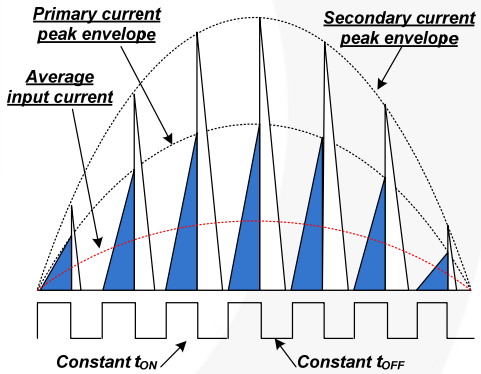


Figure 19. Power Factor Correction

Constant-Current Regulation

The output current can be estimated using the peak drain current and inductor current discharge time because output current is the same as the average of the diode current in steady state. The peak value of the drain current is determined by the CS peak voltage detector. The inductor current discharge time (t_{DIS}) is sensed by a t_{DIS} detector. With peak drain current, inductor current discharging time and operating switching period information, the TRUECURRENT® calculation block estimates output current as follows:

$$I_o = \frac{1}{2} \cdot \frac{t_{DIS}}{t_S} \cdot V_{CS} \cdot n_{PS} \cdot \frac{1}{R_S}$$

$$\frac{t_{DIS}}{t_S} \cdot V_{CS} = 0.25 \qquad (1)$$

$$I_o = 0.125 \cdot \frac{n_{PS}}{R_S}$$

where, n_{PS} is the primary-to-secondary turn ratio and R_S is a sensing resistor connected between the source terminal of the MOSFET and ground.

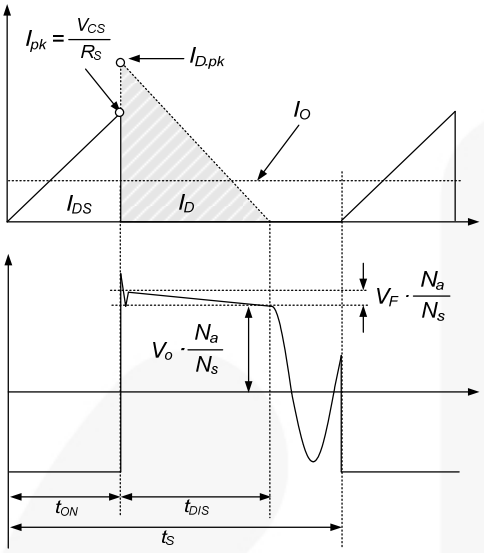


Figure 20. Key Waveforms for Primary-Side Regulation

The output of the current calculation is compared with an internal precise voltage reference to generate an error voltage (V_{COMI}), which determines the MOSFET's turn-on time in voltage-mode control. With Fairchild's innovative TRUECURRENT® technique, constant-current output can be precisely controlled.

DCM Control

As mentioned above, DCM should be guaranteed for high power factor in flyback topology. To maintain DCM across a wide range of output voltage, the switching frequency is linearly adjusted by the output voltage in linear frequency control. Output voltage is detected by the auxiliary winding and the resistive divider connected to the VS pin, as shown in Figure 21. When the output voltage decreases, secondary diode conduction time is increased and the DCM control lengthens the switching period, which retains DCM operation over the wide output voltage range, as shown in Figure 22. The frequency control lowers the primary rms current with better power efficiency in full-load condition.

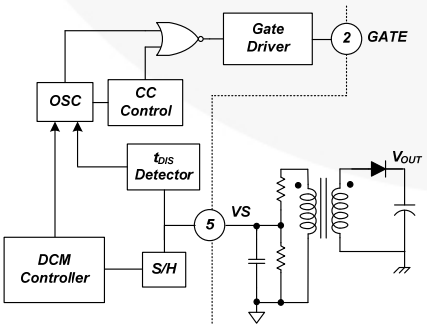


Figure 21. DCM and BCM Control

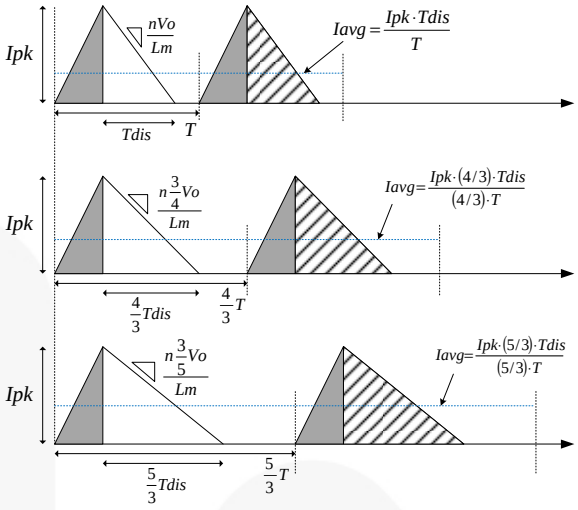


Figure 22. Primary and Secondary Current

BCM Control

The end of secondary diode conduction time could possibly be behind the end of a switching period set by DCM control. In this case, the next switching cycle starts at the end of secondary diode conduction time since FL7733 doesn't allow CCM. Consequently, the operation mode changes from DCM to BCM.

Short-LED Protection (SLP)

In case of a short-LED condition, the secondary diode is stressed by high current. When V_S voltage is lower than 0.3 V due to a short-LED condition, the cycle-by-cycle current limit level changes to 0.2 V from 1.0 V and SLP is triggered if the V_S voltage is less than 0.3 V for four (4) consecutive switching cycles. Figure 23 and Figure 24 show the SLP block and operational waveforms during LED-short condition. To set enough auto-restart time for system safety under protection conditions, V_{DD} is maintained between 13 V and 19 V, which is higher than UVLO, for 250 ms after V_{DD-ON}. SLP is disabled for an initial 15 ms to ensure successful startup in normal LED condition.

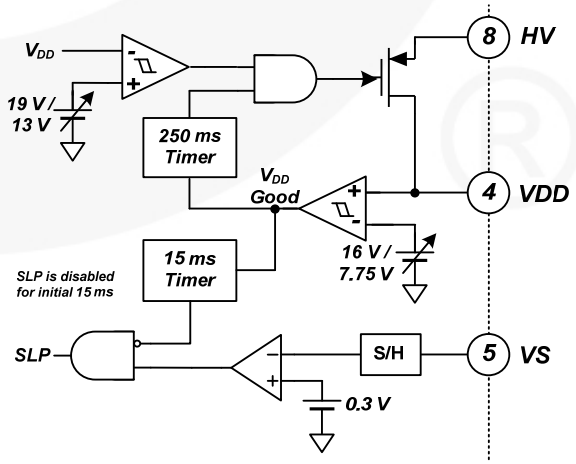


Figure 23. Internal SLP Block

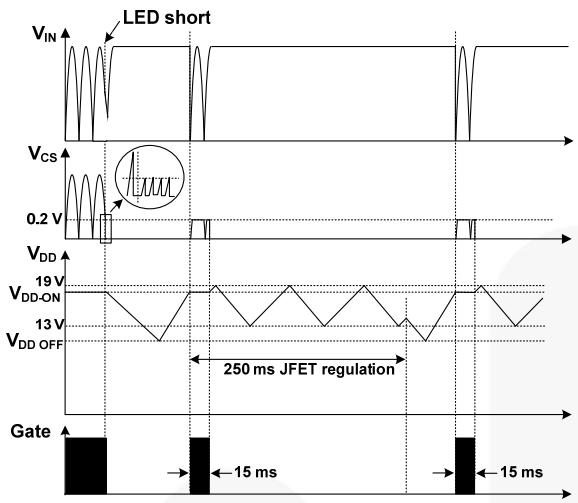


Figure 24. Waveforms in Short-LED Condition

Open-LED Protection

FL7733 protects external components, such as output diodes and output capacitors, during open-LED condition. During switch turn-off, the auxiliary winding voltage is applied as the reflected output voltage. Because the V_{DD} and V_S voltages have output voltage information through the auxiliary winding, the internal voltage comparators in the VDD and VS pins can trigger output Over-Voltage Protection (OVP), as shown in Figure 25 and Figure 26.

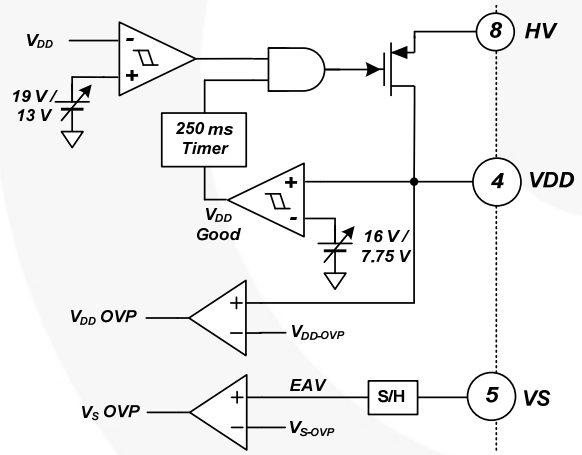


Figure 25. Internal OVP Block

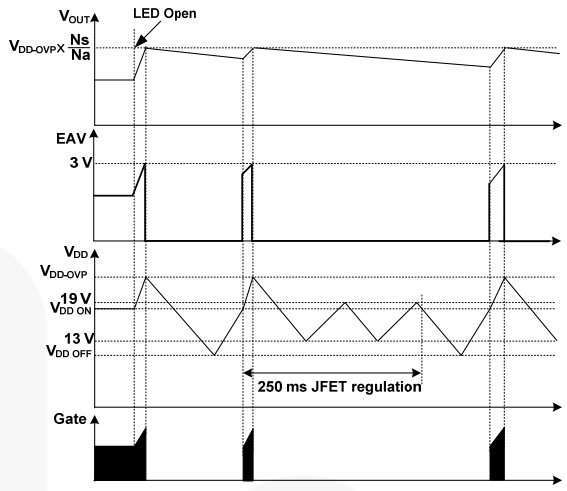


Figure 26. Waveforms in LED Open Condition

Sensing Resistor Short Protection (SRSP)

In a sensing resistor short condition, the V_{CS} level is almost zero and pulse-by-pulse current limit or OCP is not effective. The FL7733 is designed to provide sensing resistor short protection for both current and voltage mode operation. If the V_{CS} level is less than 0.1 V in the first switching cycle, the GATE output is stopped by current-mode SRSP. After 20 ms startup time, the GATE is shut down by the voltage-mode SRSP if V_{CS} level is less than 0.1 V at over 60% level of peak V_{IN}.

Under-Voltage Lockout (UVLO)

The V_{DD} turn-on and turn-off thresholds are fixed internally at 16 V and 7.75 V, respectively. During startup, the V_{DD} capacitor must be charged to 16 V through the high-voltage JFET to enable the FL7733. The V_{DD} capacitor continues to supply V_{DD} until auxiliary power is delivered from the auxiliary winding of the main transformer. V_{DD} should remain higher than 7.75 V during this startup process. Therefore, the V_{DD} capacitor must be adequate to keep V_{DD} over the UVLO threshold until the auxiliary winding voltage is above 7.75 V.

Over-Current Protection (OCP)

When an output diode or secondary winding are shorted, switch current with extremely high di/dt can flow through the MOSFET even by minimum turn-on time. The FL7733 is designed to protect the system against this excessive current. When the CS voltage across the sensing resistor is higher than 1.35 V, the OCP comparator output shuts down GATE switching.

In a sensing resistor open condition, the sensing resistor voltage can't be detected and output current is not regulated properly. If the sensing resistor is damaged open-circuit, the parasitic capacitor in the CS pin is charged by internal CS current sources. Therefore, the V_{CS} level is built up to the OCP threshold voltage and then switching is shut down immediately.

Over-Temperature Protection (OTP)

The temperature-sensing circuit shuts down PWM output if the junction temperature exceeds 150°C. The hysteresis temperature after OTP triggering is 10°C.

PCB Layout Guidance

PCB layout for a power converter is as important as circuit design because PCB layout with high parasitic inductance or resistance can lead to severe switching noise with system instability. PCB should be designed to minimize switching noise into control signals.

1. The signal ground and power ground should be separated and connected only at one position (GND pin) to avoid ground loop noise. The power ground path from the bridge diode to the sensing resistors should be short and wide.
2. Gate-driving current path (GATE – R_{GATE} – MOSFET – R_{CS} – GND) must be as short as possible.
3. Control pin components; such as C_{COMI}, C_{VS}, and R_{VS2}; should be placed close to the assigned pin and signal ground.
4. High-voltage traces related to the drain of MOSFET and RCD snubber should be kept far way from control circuits to avoid unnecessary interference.
5. If a heat sink is used for the MOSFET, connect this heat sink to power ground.
6. The auxiliary winding ground should be connected closer to the GND pin than the control pin components' ground.

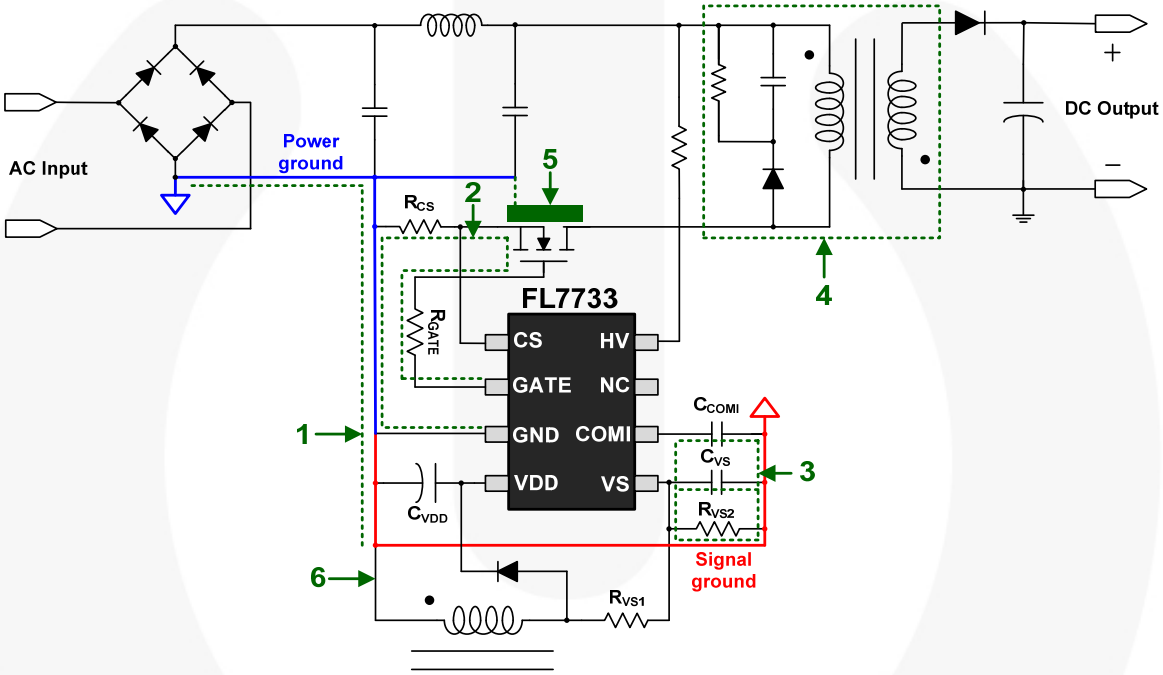
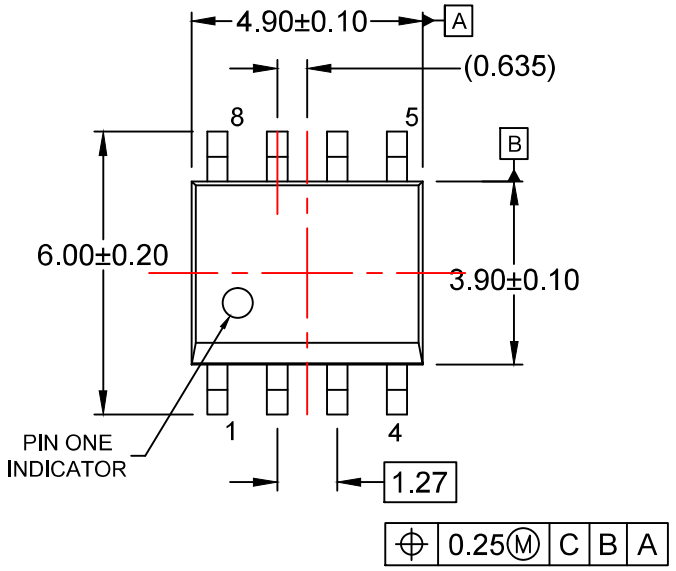
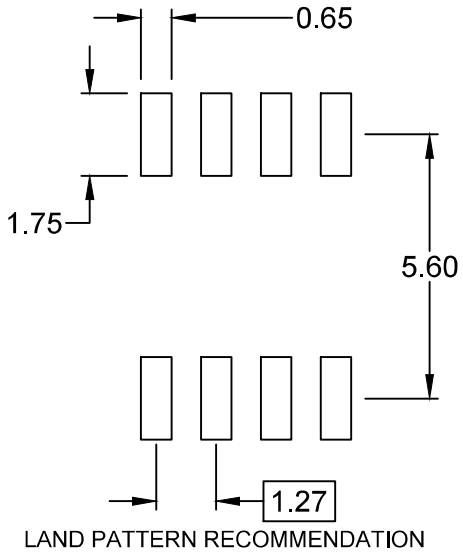
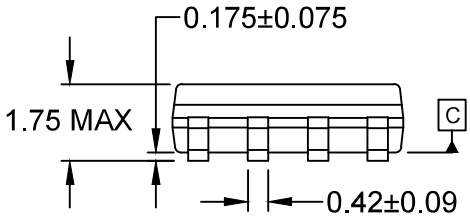


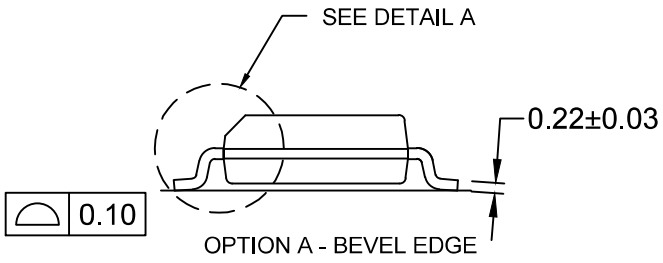
Figure 27. Layout Example



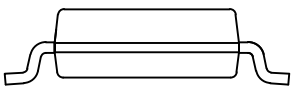


LAND PATTERN RECOMMENDATION

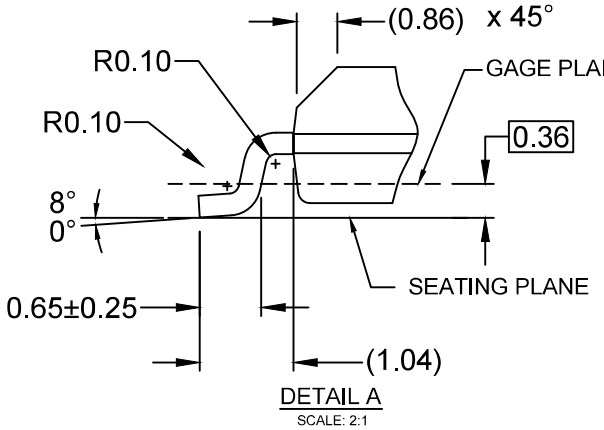




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
E) DRAWING FILENAME: M08Arev16

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